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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,085	06/30/2003	Yong-Sup Hwang	8733.873.00-US	8100

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EXAMINER	
CHOWDHURY, TARIFUR RASHID	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,085	HWANG ET AL.	
	Examiner	Art Unit	
	Tarifur R. Chowdhury	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/05/2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, USPAT 6,043,511 in view of Choi et al., (Choi), US 2002/0117691 and further in view of applicant's admitted prior art (AAPA).

4. Kim discloses and shows in Figs. 9-11 and 13A-13C, an array substrate for use in a liquid crystal display device, comprising:

- a gate electrode (12), a gate line (11) and a gate pad electrode (13) on a substrate (100), wherein all of the gate electrode, the gate line and the gate pad electrode have a double-layered structure including a first and second layers formed by AL-Nd and Mo, or Cr (first barrier metal layer) and Al-Nd (Fig. 13A; col. 6, lines 19-60);

- a gate insulating layer (20) on the substrate covering the double-layered gate electrode, gate line and gate pad (Fig. 13A);

- an active layer (30) and an ohmic contact layer (40) sequentially formed on the gate insulating layer and over the gate electrode;

- a data line (51) on the gate insulating layer crossing the gate line (11), source and drain electrodes (52, 53) contacting the ohmic contact layer (40), and a data pad electrode (54) on the gate insulating layer (Fig. 13B);

- a passivation layer (60)formed on the gate insulating layer to cover the data line, source and drain electrodes and data pad electrode, wherein the passivation layer has a drain contact hole exposing the drain electrode (53), a gate pad contact hole exposing the gate pad electrode (13), and a data pad contact hole exposing the data pad (54) (Fig. 13C) ; and

- a pixel electrode (70), a gate pad terminal and a data pad terminal all of which

are formed of a transparent conductive material on the passivation layer (col. 7, lines 18-21).

As discussed above Kim discloses that the gate electrode, gate line and gate pad electrode have double-layered structure including a first barrier metal layer and a first layer of Al-Nd. Kim differs from the instant invention because he does not explicitly disclose the limitations such as (1) the gate electrode, the gate line and the gate pad electrode have a double-layered structure wherein the first layer is copper and (2) the data line, the source and drain electrodes and the data pad electrode having a double-layered structure including a second barrier metal layer and a second copper layer.

Choi discloses an array substrate for use in a liquid crystal display device wherein the gate line assembly (including gate line, gate electrode and gate pad) and the data line assembly (includes data line, source electrode, drain electrode and data pad) can be formed of a double-layered structure such as a barrier metal layer and a copper layer. Choi also discloses that copper has low resistance(page 8, paragraph 0118; page 9, paragraph 0125, 0129, 0132-0135; page 10, paragraph 0148; page 11, paragraph 0152).

Choi is evidence that ordinary workers in the art would find a reason, suggestion or motivation to use copper to form gate line assembly and data line assembly.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the Al-Nd layer of the gate electrode, the gate line, the gate pad, the data line, the drain electrode, the source electrode and the

data pad electrode of Kim with a copper layer for advantages such as to obtain low resistance wiring, as per the teachings of Choi.

Still lacking is the limitation such as the first barrier metal layer and the first copper layer having a smooth taper shape without any steps on their sides.

The AAPA described in the instant application is also related to an array substrate for use in a liquid crystal display device wherein the first and second metal patterns (29a, 29b) have a smooth taper shape without any steps on their sides (Fig. 2D). The AAPA further discloses that by having patterns having a smooth taper shape without any steps on their sides prevent deposition defects caused by overhang phenomenon (page 6, paragraph's 0015-0016).

The AAPA is evidence that ordinary workers in the art would find a reason, suggestion or motivation to have a smooth taper shape without any steps on their sides for the first and second metal layers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to make the first barrier metal layer and the first copper layer into a smooth taper shape without any steps on their sides to prevent deposition defects caused by overhang phenomenon, as per the teachings of the AAPA.

Accordingly, claim 1 would have been obvious.

As to claim 17, the method of forming the array substrate for use in a liquid crystal display device merely recites the steps of forming each element and since each element must be formed to make the device, the method would have at least been obvious.

As to claims 2, 3, 18 and 19, Kim shows in Fig. 9 that the gate electrode (12) extends from the gate line (11) and the gate electrode is at the end of the gate line and that the source electrode (52) extends from the data line (51), wherein the drain electrode (53) is spaced apart from the source electrode, and wherein the data pad (54) is at the end of the data line (51).

As to claims 4 and 20, Figs. 9 and 13C of Kim also shows that the pixel electrode (70) is disposed in a pixel region defined by the crossing of the gate and data lines, wherein the pixel electrode contacts the drain electrode (53) through the drain contact hole, wherein the gate pad terminal contacts the gate pad through the gate pad contact hole (14) and wherein the data pad terminal contacts the data pad through the data pad contact hole (55).

As to claims 5-8 and 21-24, Kim discloses that the barrier metal layer is chromium, which inherently has good adhesive characteristics (col. 6, lines 56-60).

As to claims 9, 10, 25 and 26, Choi discloses (page 6, paragraph 0091) and shows in Fig. 7, a double-layered capacitor electrode on the gate insulating layer and over the portion of the gate line, wherein the double-layered capacitor electrode is connected in parallel with the pixel electrode through a contact hole that formed in the passivation layer and thus would have been obvious to form storage capacitance for improving storage capacity of the pixel electrode.

As to claims 11 and 27, Kim discloses (col. 4, lines 66-67) that the gate insulation layer is an inorganic material such as silicon oxide or silicon nitride.

As to claims 12 and 28, Kim further discloses (col. 5, lines 14-15) that the passivation layer is made of silicon nitride.

As to claims 13-16 and 29-32, Choi discloses the use of a buffer layer (page 9, paragraph 0131) made of an inorganic material to separate the gate line assembly from the substrate and data line assembly form the thin film transistor array to prevent contacts between the substrate and the barrier metal layer as well as the contacts between the barrier metal layer and the thin film transistor array and thus would have been obvious.

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

USPAT 6,362,507 and US 2003/0169380 also shows gate electrode with double-layered structure having tapered shape without any steps on its sides.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R. Chowdhury whose telephone number is (571) 272-2287. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRC
January 14, 2006

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER